



# BCT646

## 2:1 MIPI D-PHY(2.5Gbps) 4-Data Lane Switch

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### GENERAL DESCRIPTION

The BCT646 is a four-data-lane, MIPI, D-PHY switch. This single-pole, double-throw (SPDT) switch is optimized for switching between two high-speed or low-power MIPI sources. The BCT646 is designed for the MIPI specification and allows connection to a CSI or DSI module.

### APPLICATIONS

Cellular Phones, Smart Phones  
Displays  
Tablets  
Laptops

### FEATURES

Switch Type: SPDT(10x)  
Signal Types: MIPI, D-PHY  
 $V_{CC}$ : 1.5 to 5.0V  
Input Signals: 0 to 1.3V  
 $R_{ON}$ : 7                    HS MIPI  
7                    LP MIPI  
 $R_{ON}$ : 0.15    Typical HS &LP MIPI  
 $R_{ON\_FLAT}$ : 0.2  
 $I_{CCZ}$ : 1uA Maximum  
 $I_{CC}$ : 35uA Maximum  
 $O_{IRR}$ : -25dB Typical  
 $X_{TALK}$ : -30dB Typical  
Bandwidth: 2.5 GHz Typical  
Channel-to-Channel Skew: 6ps Typical  
 $C_{ON}$ : 1.5pF  
36-Ball WLCSP Package





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### ABSOLUTE MAXIMUM RATINGS

Supply Voltage ( $V_{CC}$ )	.....-0.5V to +6.0V
DC Input Voltage (SEL, /OE) <sup>(1)</sup>	.....-0.5V to $V_{CC}$ V
DC Switch I/O Voltage	.....-0.5V to 1.8V
DC Input Diode Current	.....-50mA
DC Output Current	.....25mA
Storage Temperature Range	.....-65 to +150
Junction Temperature	.....150
Operating Temperature Range	.....-40 to +85
Lead Temperature (Soldering, 10 sec)	.....260
ESD Susceptibility	
HBM All Pins	.....2.0KV
CDM	.....1KV
IEC 61000-4-2 System (Contact)	.....8KV
IEC 61000-4-2 System (Air Gap)	.....15KV

### CAUTION

pay attention to ESD protection. Broadchip recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Broadchip reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time. Please contact Broadchip sales office to get the latest datasheet.

### RECOMMENDED OPERATING CONDITONS

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications.

Symbol	Parameter	Min.	Max.	Unit	
$V_{CC}$	Supply Voltage	1.5	5.0	V	
$V_{CTRL}$	Control Input Voltage(SEL, /OE) <sup>(2)</sup>	0	$V_{CC}$	V	
$V_{SW}$	Switch I/O Voltage (CLKn, CLKA <sub>n</sub> , CLKB <sub>n</sub> , Dn, DAN, DBn)	HS Mode	0	0.3	V
		LP Mode	0	1.3	
$T_A$	Operating Temperature	-40	+85		

#### Notes

- The input and output negative ratings maybe exceed if the input and output diode current ratings are observed.
- The control input must be held HIGH or LOW; it must not float.

**PIN CONFIGURATION**

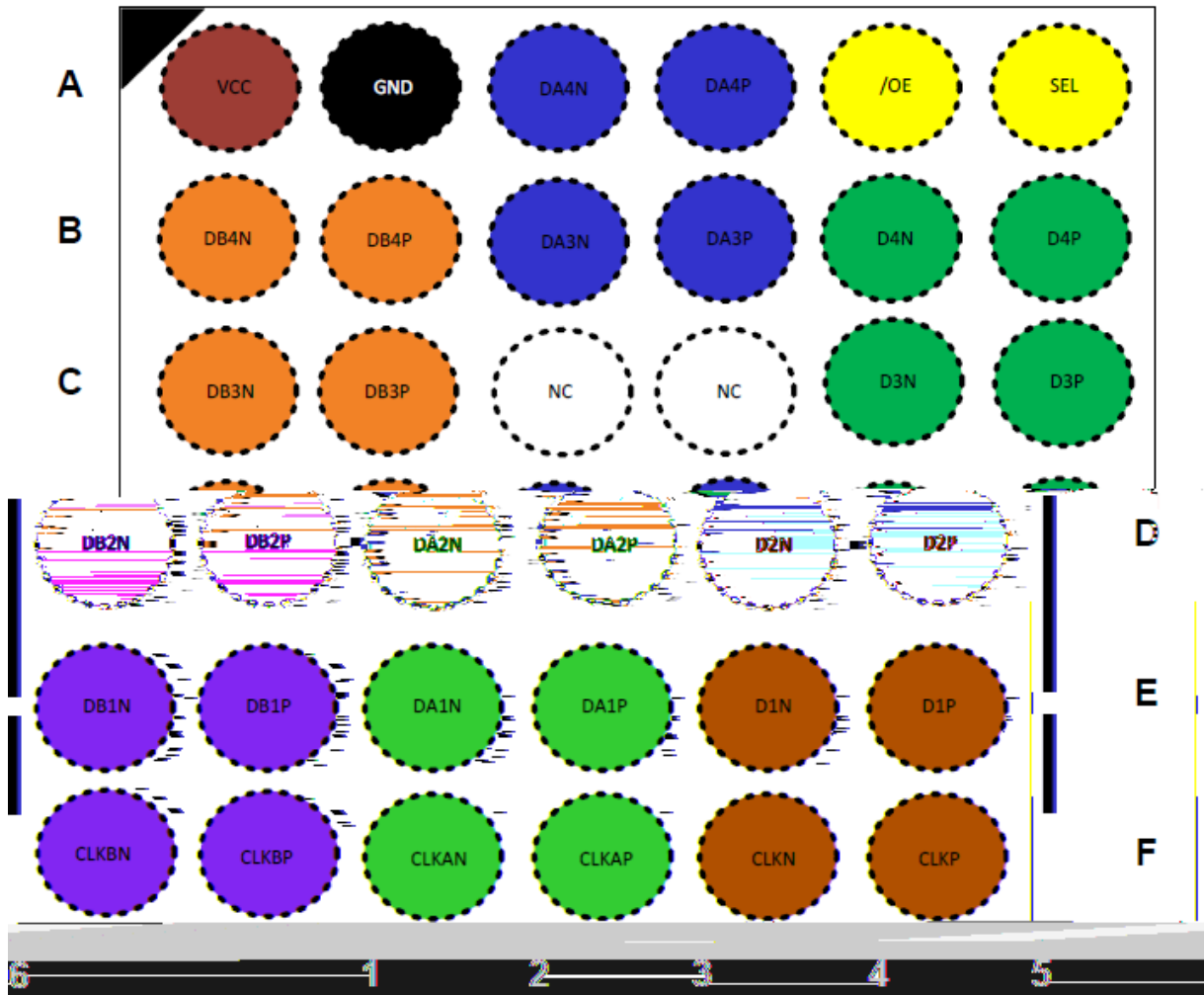


Figure2. Pin Configuration(Top Through View)



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**Table 1. Ball-to-Pin Mappings**

<b>Ball</b>	<b>Pin Name</b>
A1	V <sub>CC</sub>
A2	GND
A3	DA4N
A4	DA4P
A5	/OE
A6	SEL
B1	DB4N
B2	DB4P
B3	DA3N
B4	DA3P

### PIN DESCRIPTION

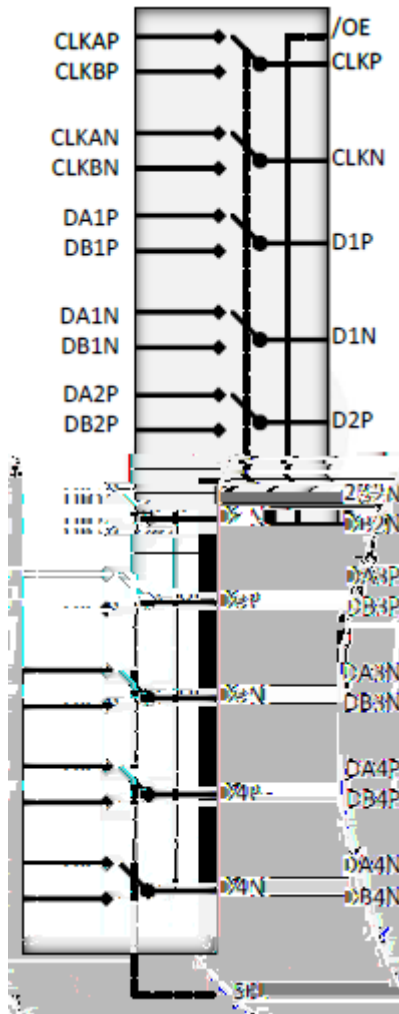


Figure 3. Analog Symbol

Pin Name	Description	
CLKP/N	Common Clock Path	
D1P/N	Common Data Path1	
D2P/N	Common Data Path2	
D3P/N	Common Data Path3	
D4P/N	Common Data Path4	
CLKAP/N	A-Side Clock Path	
DA1P/N	A-Side Data Path 1	
DA2P/N	A-Side Data Path 2	
DA3P/N	A-Side Data Path 3	
DA4P/N	A-Side Data Path 4	
CLKBP/N	B-Side Clock Path	
DB1P/N	B-Side Data Path 1	
DB2P/N	B-Side Data Path 2	
DB3P/N	B-Side Data Path 3	
DB4P/N	B-Side Data Path 4	
SEL	SEL=0	CLKP=CLKAP, CLKN=CLKAN, Dn(P/N)=DAn(P/N)
	SEL=1	CLKP=CLKBP, CLKN=CLKBN, Dn(P/N)=DBn(P/N)
/OE	Output Enable	
VCC	Power	
GND	Ground	
NC	No Connect	



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### DC ELECTRICAL CHARACTERISTICS

( All typical values are  $T_A = 25$  , unless otherwise specified.)

PARAMETER	SYM	CONDITIONS	V <sub>CC</sub> (V)	MIN	TYP	MAX	UNITS
Control Input Leakage(SEL, /OE)	I <sub>IN</sub>	V <sub>CNTRL</sub> =0 to V <sub>CC</sub>	5	-1		1	uA
Input Voltage High	V <sub>IH</sub>	SEL, /OE	1.5 to 5	1.4			V
Input Voltage Low	V <sub>IL</sub>	SEL, /OE	1.5 to 5			0.4	V
Off leakage Current of Port CLKAn, DAN, CLKBn, DBn	I <sub>NO(OFF)</sub> I <sub>NC(OFF)</sub>	V <sub>SW</sub> =0 DATA 1.3V	5	-1		1	uA
On leakage Current of Common Ports(CLK <sub>n</sub> , D <sub>n</sub> )	I <sub>A(ON)</sub>	V <sub>SW</sub> =0 DATA 1.3V	5	-1		1	uA
Power-Off Leakage Current (All I/O Ports)	I <sub>OFF</sub>	V <sub>SW</sub> =0 or 1.3V	0	-1		1	uA
Off-State Leakage	I <sub>OZ</sub>	V <sub>SW</sub> =0 DATA 1.3V, /OE=High	5	-1		1	uA
Switch On Resistance for HS MIPI Applications <sup>(3)</sup>	R <sub>ON_MIPI_HS</sub>	I <sub>ON</sub> =-8mA, /OE=0V, SEL=V <sub>CC</sub> or 0V, CLKA, CLKB, DBn or DAN=0.3V	1.5 to 5		7		
Switch On Resistance for LP MIPI Applications <sup>(3)</sup>	R <sub>ON_MIPI_LP</sub>	I <sub>ON</sub> =-8mA, /OE=0V, SEL=V <sub>CC</sub> or 0V, CLKA, CLKB, DBn or DAN=1.3V	1.5 to 5		7		
On Resistance Matching Between HS MIPI Channels <sup>(4)</sup>	R <sub>ON_MIPI_HS</sub>	I <sub>ON</sub> =-8mA, /OE=0V, SEL=V <sub>CC</sub> or 0V, CLKA, CLKB, DBn or DAN=0.3V	1.5 to 5		0.15		

### DC ELECTRICAL CHARACTERISTICS



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## 2:1 MIPI D-PHY(2.5Gbps) 4-Data Lane Switch

( All typical values are  $T_A = 25^\circ\text{C}$  , unless otherwise specified.)

PARAMETER	SYM	CONDITIONS	V <sub>CC</sub> (V)	MIN	TYP	MAX	UNITS
On Resistance Matching Between LP MIPI Channels <sup>(4)</sup>	R <sub>ON_MIPI_LP</sub>	I <sub>ON</sub> =-8mA, /OE=0V, SEL=V <sub>CC</sub> or 0V, CLKA, CLKB, DBn or DAN=1.3V	1.5 to 5		0.15		
On Resistance Flatness for HS MIPI Signals <sup>(4)</sup>	R <sub>ON_FLAT_MIPI_HS</sub>	I <sub>ON</sub> =-8mA, /OE=0V, SEL=V <sub>CC</sub> or BT1 0 0 1 4					





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## 2:1 MIPI D-PHY(2.5Gbps)

### 4-Data Lane Switch

## AC ELECTRICAL CHARACTERISTICS

( All values are for  $V_{CC}=3.3V$  at  $T_A=25$  unless otherwise specified.)

PARAMETER	SYM	CONDITIONS	$V_{CC}$ (V)	MIN	TYP	MAX	UNITS
Turn-Off Time SEL to Output	$t_{OFF}$	$R_L=$ , $C_L=0pF$ , $V_{SW}=0.6V$	1.5 to 5		125	800	ns
Break-Before-Make Time	$t_{BBM}$	$R_L=$ , $C_L=0pF$ , $V_{SW}=0.6V$	1.5 to 5	50		450	ns
Propagation Delay <sup>(5)</sup>	$t_{PD}$	$C_L=0pF$ , $R_L=$	1.5 to 5		0.25		ns
Off Isolation for MIPI <sup>(5)</sup>	$O_{IRR}$	$f=1250MHz$ , $R_L=$ , $/OE=HIGH$ , $V_{SW}=200mV_{PP}$	1.5 to 5		-25		dB
Crosstalk for MIPI <sup>(5)</sup>	$X_{TALK}$	$f=1250MHz$ , $R_L=$ , $/OE=High$ , $V_{SW}=200mV_{PP}$	1.5 to 5		-30		dB
		$f=1250MHz$ , $R_L=$ , $/OE=Low$ , $V_{SW}=200mV_{PP}$	1.5 to 5		-30		dB
-3db Bandwidth <sup>(5)</sup>	BW	$C_L=0pF$ , $R_L=$ , $V_{SW}=200mV_{PP}$	1.5 to 5		2.5		GHz

**Note:**

5. Guaranteed by characterization.

## HIGH-SPEED-RELATED AC ELECTRICAL CHARACTERISTICS

PARAMETER	SYM	CONDITIONS	$V_{CC}$ (V)	MIN	TYP	MAX	UNITS
HS Mode Skew of Opposite Transitions of the Same Output <sup>(6)</sup>	$t_{SK(P)}$	$R_L=$ , $C_L=0pF$ , $V_{SW}=0.3V$	1.5 to 5		6		ps

**Note:**

6. Guaranteed by characterization.

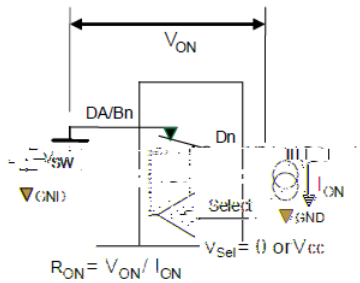
## CAPACITANCE

PARAMETER	SYM	CONDITIONS	$V_{CC}$ (V)	MIN	TYP	MAX	UNITS
Control Pin Input Capacitance <sup>(7)</sup>	$C_{IN}$	$V_{CC}=0V$ , $f=1MHz$	0		2.1		pF
Output On Capacitance <sup>(7)</sup>	$C_{ON}$	$V_{CC}=3.3V$ , $/OE=0V$ , $f=1250MHz$ (In HS common value)	3.3		1.5		
Output Off Capacitance <sup>(7)</sup>	$C_{OFF}$	$V_{CC}$ and $/OE=3.3V$ , $f=1250MHz$ (Both sides in HS common value)	3.3		0.9		

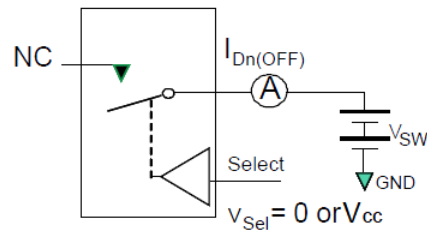
**Note:**

7. Guaranteed by characterization.

### TEST DIAGRAMS

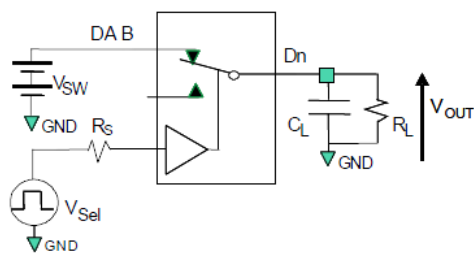


**Figure 4. On Resistance**



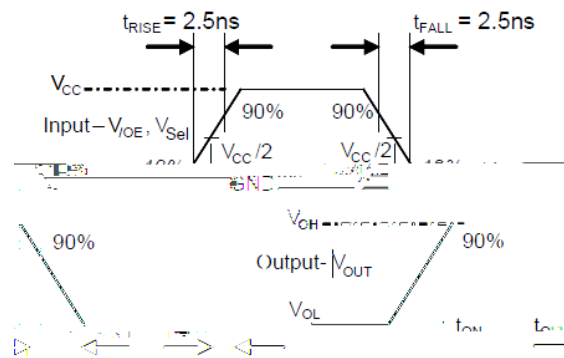
\*\*Each switch port is tested separately

**Figure 5. Off Leakage**

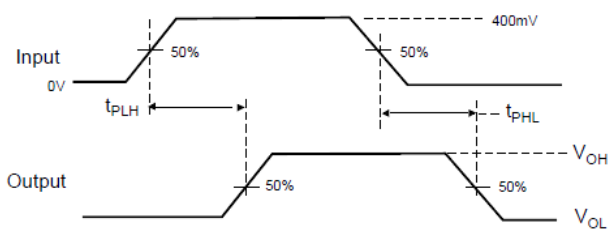


$R_L$ ,  $R_S$ , and  $C_L$  are functions of the application environment (see AC Tables for specific values).  $C_L$  includes test fixture and stray capacitance.

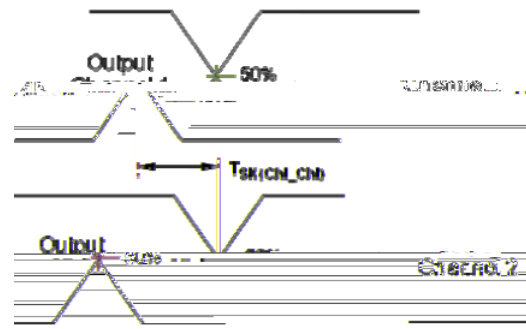
**Figure 6. AC Test Circuit Board**



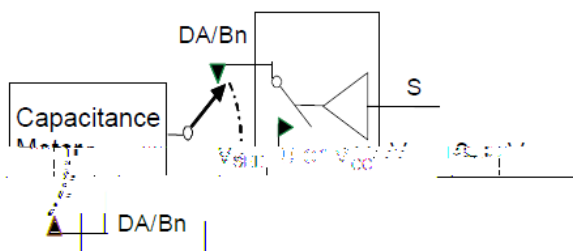
**Figure 7. Turn-On/Turn-Off waveform**



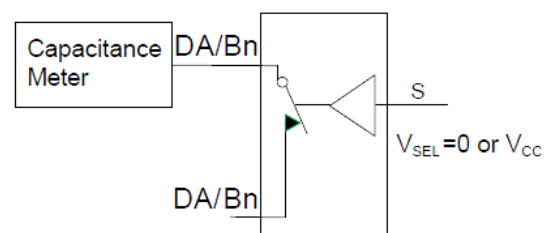
**Figure 8. Propagation Delay ( $t_{R/F} < 500ps$ )**



**Figure 9. Channel to Channel Skew**

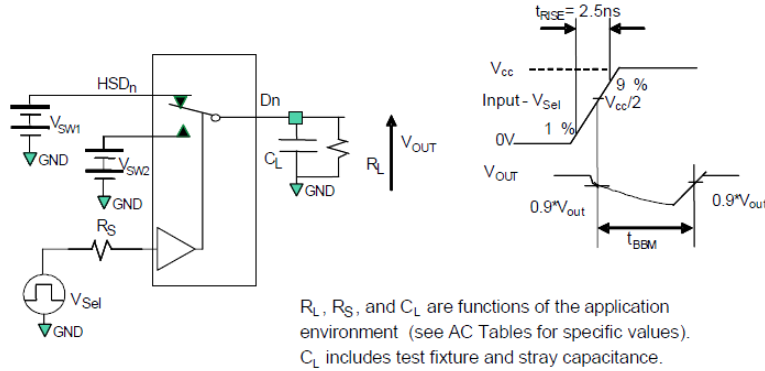


**Figure 10. Channel Off Capacitance**

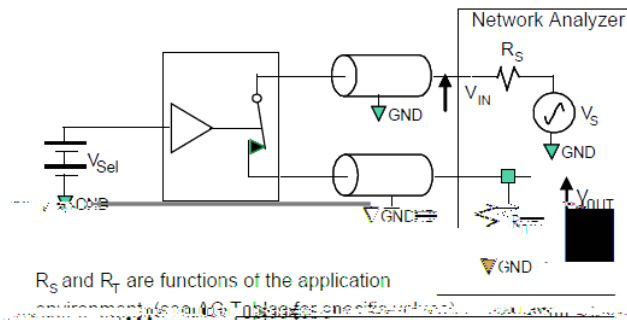


**Figure 11. Channel On Capacitance**

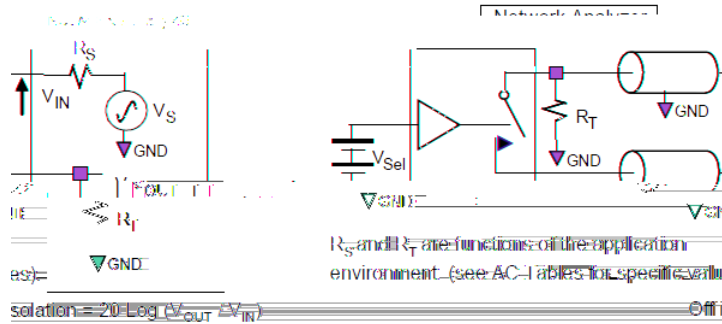
## TEST DIAGRAMS(CONTINUED)



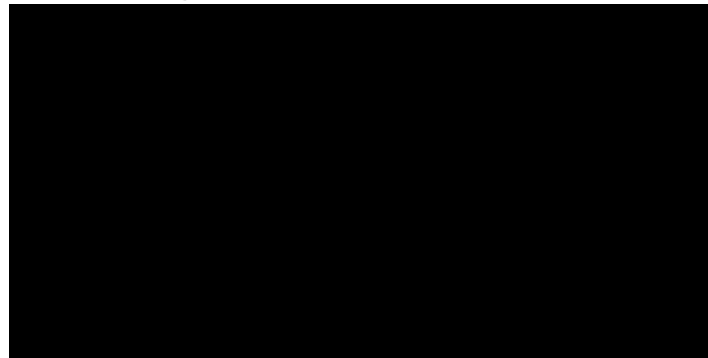
**Figure 12. Break-Before-Make Interval Timing**



**Figure 13. Bandwidth**

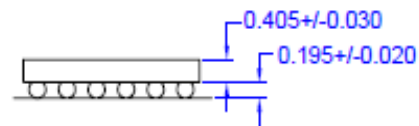
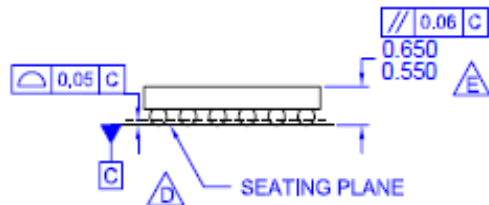
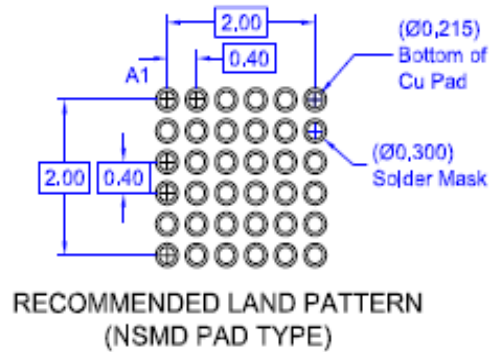
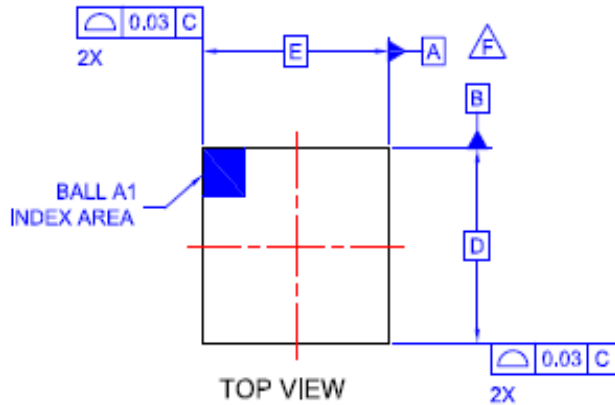


**Figure 14. Channel Off Isolation**



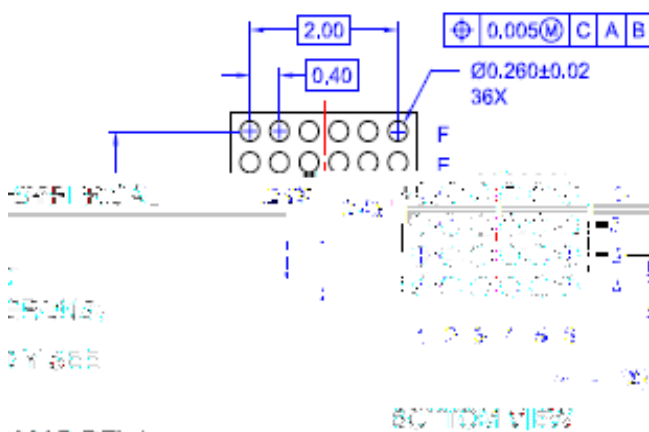
**Figure 15. Non-Adjacent Channel-to-Channel Crosstalk**

### PACKAGE OUTLINE DIMENSIONS



#### NOTES

- A. NO JEDEC REGISTRATION APPLIES.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCE PER ASMEY14.5M, 2009.



- D. OUTLINE IS DERIVED FROM CROWTHER 01-FF-0415
- E. PACKAGE TERMINAL FINISHING PER JEDEC STANDARD J-ESD-020
- F. FOR DIMENSIONS D, E, X, AND Y, SEE PRODUCT DATASHEET.
- G. DRAWING FILENAME: MKT-UC0

#### Product-Specific Dimensions

Product	Package	D	E	X	Y
BCT646EWX-TR	36-Ball WLCSP, 2.43mm x 2.43 mm, 0.4mm Pitch	2.43mm	2.43mm	0.18mm	0.18mm